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| 09/591,270 | 06/09/2000 | Kenneth Shepard | AP32158-070050.1280 | 2448 |

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BAKER & BOTTS
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

| EXAMINER | |
|---|---|
| SHARON, AYAL I | |

| ART UNIT | PAPER NUMBER |
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| 2123 | |

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/591,270 | SHEPARD, KENNETH | |
| | Examiner | Art Unit | |
| | Ayal I Sharon | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 1-22 of U.S. Application 09/591,270 originally filed on 06/09/2000 are presented for examination.
2. Examiner finds Applicant's Declaration Pursuant to 37 C.F.R. §1.131, filed 12/4/2003, to be defective.
3. Moroever, Examiner raised issues in a Requirement to Submit Information 37 C.F.R. §1.105, dated 2/24/2004. Examiner finds that Applicant's Response, filed on 6/28/2004, to this §1.105 requirement, did not sufficiently respond to the issues.
4. These problems are discussed in detail in the "Re: Applicant's Response to §1.105" and "Re: Applicant's 37 C.F.R. §1.131 Declaration" sections of this Office Action.
5. The claim rejections are therefore maintained.

### *Drawings*

6. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Figures 1-13 have handwritten labels, and Figure 7 is handwritten in its entirety.

### *Allowable Subject Matter*

7. Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims. The allowable limitation is that of Claim 9:

> 9. The method of claim 6, further comprising the step of performing active net tagging, after said checking step, on each of said one or more nets to determine whether any of said one or more nets will switch with regular frequency.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. The prior art used for these rejections is as follows:

10. Chuang et al., U.S. Patent Application Publication No. US 2003 / 0078763 A1. Filed: April 19, 1999. (Henceforth referred to as "**Chuang**").

11. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

12. **Claims 1-4 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang.**

13. In regards to Claim 1, Chuang teaches the following limitations:

1 . A method for statically estimating a body voltage of one or more transistors which form digital partially depleted silicon-on-insulator circuit having a predetermined circuit topology comprising said one or more transistors and one or more nets connecting said transistors, comprising the steps of:

a. obtaining one or more device models, each corresponding to one of said one or more transistors;
(Chuang, especially: Fig.I and associated text)

b. abstracting each of said device models to generate one or more simplified electrical descriptions, each corresponding to one of said one or more transistors;
(Chuang, especially: Fig.3 and associated text)

c. checking said predetermined circuit topology to generate one or more sets of accessible states, each set corresponding to one of said one or more transistors and being indicative of whether under any allowable switching activity, the source, gate or drain could be high or low.
(Chuang, especially: Fig.2 and associated text)

d. determining one or more sets of reference state body voltage minima and reference state body voltage maxima, one for each of said one or more transistors, based on corresponding simplified electrical descriptions and corresponding sets of accessible states; and
(Chuang, especially: Fig.6 and associated text)

e. ascertaining one or more target state body voltage minima and target state body voltage maxima, one for each of said one or more transistors, based on said determined sets of reference state body voltage minima and reference state body voltage maxima.
(Chuang, especially: Fig.6 and associated text)

14. In regards to Claim 2, Chuang teaches the following limitations:

2. The method of claim 1, wherein said device models are selected from the group consisting of an n channel Field Effect Transistor model and a p channel Field Effect Transistor model.
(Chuang, especially: Fig.5 and associated text)

15. In regards to Claim 3, Chuang teaches the following limitations:

3. The method of claim 2, wherein said abstracting step comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more displacement voltages $d_i$, and one or more steady-state reference voltages $V_i^{zero}$ for each of said device models.
(Chuang, especially: p.3, para. 58-67.)

16. In regards to Claim 4, Chuang teaches the following limitations:

4. The method of claim 3, wherein said corresponding simplified electrical descriptions

comprise said displacement voltages di, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages di, and corresponding set of accessible states.
(Chuang, especially: p.3, para. 58-67.)

17. In regards to Claim 16, Chuang teaches the following limitations:

16. A method for analyzing an electrical property of a digital partially depleted silicon-on insulator circuit having a predetermined circuit topology comprising one or more transistors and one or more nets, comprising the steps of:

a. ascertaining a target state body voltage minimum and a target state body voltage minimum for each of said transistors in said circuit;
(Chuang, especially: Fig.6, and associated text)

b. establishing an initial condition for said circuit by selecting either said target state body voltage minimum or said target state body voltage minimum for each of said transistors In said circuit;
(Chuang, especially: Fig.6, and associated text)

c. applying a voltage to said circuit; and
(Chuang, especlally'. Fig.6, Item 57 and associated text)

d. measuring said electrical property of said circuit.
(Chuang, especially: Fig.6, Item 57 and associated text)

18. In regards to Claim 17, Chuang teaches the following limitations:

17. The method of claim 16, wherein said electrical property comprises a switching delay and said measuring step comprises measuring a delay between a switching input and a switching output as a constituent simulation for static timing analysis.
(Chuang, especially: pp.3-4, para. 68-71)

## *Claim Rejections - 35 USC § 103*

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The prior art used for these rejections is as follows:

21. Chuang et al., U.S. Patent Application Publication No. US 2003 / 0078763 A1. Filed: April 19, 1999. (Henceforth referred to as "**Chuang**").

22. Shepard, K.L. et al. "Body-Voltage Estimation in Digital PD-SOI Circuits and Its Application to Static Timing Analysis". 1999 IEEE/ACM Int'l Conf. on CAD. Nov. 7-11, 1999. pp.531-538. (Henceforth referred to as "**Shepard**").

23. Shepard, K.L. et al. "Harmony: Static Noise Analysis of Deep Submicron Digital Integrated Circuits". 1999 IEEE Transactions on CAD of Integrated Circuits and Systems. August, 1999. pp.1132-1150. (Henceforth referred to as "**Shepard_2**").

24. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

25. **Claims 5-8, 12-15 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chuang in view of Shepard.**

26. In regards to Claim 5, Chuang teaches initializing body potential to either the highest or lowest values in a range (see Fig.6, and associated text).

However, Chuang does not expressly teach the use of "uncertainty estimation" as claimed in the following limitation'.

> 5. The method of claim 4, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using full uncertainty estimation.

Shepard, on the other hand, does expressly teach the use of "full uncertainty estimation." (see p.535, section 32.2, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because "Uncertainty is built into the timing analysis to account for variations in the effective gate input capacitance depending on the switched state of the gate (loading uncertainty)." (Shepard: p.535, Section 4, 1st para.).

27. In regards to Claim 6,

> 6. The method of claim 2, wherein said abstracting step comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models, if any, to obtain one or more displacement voltages di, steady-state Zero Forward reference voltages Vi , and forward bias reference voltages Vi for each of said device models.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach displacement voltages, steady-state reference voltages, or forward bias voltages as in the limitations, as recited in the claim limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard teaches displacement voltages (see Shepard, section 3.1, 1st para.), steady-state reference voltages (see Shepard, p.532, section 3.1, Eq.3; and p.533, col.1, para. 2), and forward bias voltages (see Shepard, p.533, col.1, para. 2-3), as recited in the claim limitations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

28. In regards to Claim 7,

> 7. The method of claim 6, wherein said corresponding simplified electrical descriptions comprise said displacement voltages di, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages di, and corresponding set of accessible states.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach displacement voltages, reference state body voltages, or accessible states, as recited in the claim limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard teaches displacement voltages (see Shepard, p.532, section 3.1, 1st para.), reference state body voltages (see Shepard, p.532, section 3.1, Eq.3; p.533, col.1 , para. 2; and 4 types of estimation detailed in p.533: "Full-uncertainty body-voltage estimation", "Initial-condition body-voltage estimation"; "Accessibility steady-state body-voltage estimation", "Detailed steady-state body-voltage estimation"), and accessible states (see Shepard, p.533, col.1, para. 2-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1 , para.2).

29. In regards to Claim 8,

> 8. The method of claim 7, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using accessibility analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach displacement voltages, reference state body voltages, or accessible states, as recited in the limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard, teaches displacement voltages (see Shepard, p.532 section 3.1, 1st para.), reference state body voltages (see Shepard, p.532, section 3.1, Eq.3; p.533, col.1, para. 2; and p.533, col.2, "Accessibility steady-state body-voltage estimation"), and accessible states (see Shepard, p.533, col.1, para. 2-3; and p.533, col.2, "Accessibility steady-state body-voltage estimation").

It would have been obvious to one of ordinary skill in the ad at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty,

depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

30. In regards to Claim 12,

> 12. The method of claim 6, wherein said abstracting step fudher comprises abstracting each of said n channel Field Effect Transistor models, if any, and each of said p channel Field Effect Transistor models if any, to obtain one or more corresponding time constant characterizations, one for each of sald device models.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach time constant characterizations for the model devices.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard teaches modeling time constant characterizations (see Shepard p.532, section 3.1, 1st para; and p.532, col.1, 1st para.) by "simple polynomial curve fits to circuit simulation results, since the relationships are too complex to motivate physically-based formulae".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those

of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of tie FETs in question." (Shepard, p.538, col.1, para.2).

31. In regards to Claim 13,

13. The method of claim 12, further comprising the step of calculating signal probabilities and timing windows from said time constant characterizations, after said checking step, on each of said one or more nets, wherein said signal probabilities are determined by Boolean analysis, and said timing windows are determined by timing analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach time windows determined by timing analysis and signal probabilities determined by Boolean analysis.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard teaches modeling time constant characterizations (see Shepard, p.532, section 3.1, 1st para.; and p.532, col.1, 1st para.) by "simple polynomial curve fits to circuit simulation

results, since the relationships are too complex to motivate physically-based formulae". Shepard also teaches "We characterize the logical environment of each FET by a set of signal probabilities which determine the possible states of the source, gate, and drain of the transistor at the end of a cycle." (see Shepard: p.533, col.2, section 3.2, 2nd para.)

It would have been obvious to one of ordinary skill in the ad at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

32. In regards to Claim 14,

> 14. The method of claim 13, wherein said corresponding simplified electrical descriptions comprise said displacement voltages di, and said determining step comprises determining said sets of reference state body voltage minima, and reference state body voltage maxima based on corresponding displacement voltages di, corresponding sets of accessible states, and from said calculated signal probabilities and timing windows.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach displacement voltages,

reference state body voltages, or accessible states, time windows determined by timing analysis, or signal probabilities determined by Boolean analysis.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard teaches displacement voltages (see Shepard, p.532, section 3.1, 1st para.), reference state body voltages (see Shepard, p.532, section 3.1, Eq.3; p.533, col.1, para. 2; and 4 types of estimation detailed in p.533: "Full-uncertainty body-voltage estimation"; "Initial-condition body-voltage estimation"; "Accessibility steady-state body-voltage estimation", "Detailed steady-state body-voltage estimation"), and accessible states (see Shepard, p.533, col.1, para. 2-3).

Shepard also teaches modeling time constant characterizations (see Shepard p.532, section 3.1, 1st para.; and p.532, col.1, 1st para.) by "simple polynomial curve fits to circuit simulation results, since the relationships are too complex to motivate physically-based formulae". Shepard also teaches "We characterize the logical environment of each FET by a set of signal probabilities which determine the possible states of the source, gate, and drain of the transistor at the end of a cycle." (see Shepard: p.533, col.2, section 3.2, 2nd para.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

33. In regards to Claim 15,

15. The method of claim 14, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, based on said determined reference state body voltage minima and maxima using probabilistic analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach ascertaining body voltage maxima and/or minima by probabilistic analysis.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the [time] slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard also teaches "We characterize the logical environment of each FET by a set of signal probabilities which

determine the possible states of the source, gate, and drain of the transistor at the end of a cycle." (see Shepard: p.533, col.2, section 3.2, 2nd para.). Shepard also teaches: "... From these probabilities, one can calculate a set of thirty-six transition probabilities for both the minimum or maximum cases ...". (see Shepard: p.534, col.1, 1st para.).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

34. In regards to Claim 19,

19. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using full uncertainty estimation.

Chuang teaches initializing body potential to either the highest or lowest values in a range (see Fig.6, and associated text).

However, Chuang does not expressly teach the use of "uncertainty estimation".

Shepard, on the other hand, does expressly teach the use of "full uncertainty estimation." (see p.535, section 32.2, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those

of Shepard because "Uncertainty is built into the timing analysis to account for variations in the effective gate input capacitance depending on the switched state of the gate (loading uncertainty)." (Shepard: p.535, Section 4, 1st para.).

35. In regards to Claim 20,

> 20. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using accessibility analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach reference state body voltages, or accessible states, as recited in the limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the [time] slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$". (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard, teaches reference state body voltages (see Shepard, p.532, section 3.1, Eq.3; p.533, col.1, para. 2; and p.533, col.2, "Accessibility steady-state body-voltage estimation"), and accessible states (see Shepard, p.533, col.1, para.2-3; and p.533, col.2, "Accessibility steady-state body-voltage estimation").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

36. In regards to Claim 21,

21. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima and one or more target state body voltage maxima, using modified accessibility analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach reference state body voltages, or modified accessibility analysis, as recited in the limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard, teaches reference state body voltages (see Shepard, p.532, section 3.1 , Eq.3; p.533, col.1, para. 2., and p.533,

col.2, "Accessibility steady-state body-voltage estimation"). Shepard also teaches modified accessibility analysis: "The uncertainty of accessibility estimation can be reduced if one is further willing to restrict the allowable waveforms to those meeting known timing requirements and known signal probabilities" (see Shepard, p.533, col.2, "Accessibility steady-state body-voltage estimation").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

37. In regards to Claim 22,

> 22. The method of claim 16, wherein said ascertaining step comprises ascertaining one or more target state body voltage minima, and one or more target state body voltage maxima, using probabilistic analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling; and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach reference state body voltages, or probabilistic analysis, as recited in the limitations.

Shepard teaches that "In characterizing the body voltage, we choose a reference state of state 2 for the nFET and state 1 for the pFET. The discontinuities between the (time) slices occur as a result of the capacitive coupling kicks and are characterized by the voltage differences, or displacements $d_i$." (see Shepard: p.532, col.2, section 3.1, 1st para.).

More specifically, Shepard, teaches reference state body voltages (see Shepard, p.532, section 3.1, Eq.3; p.533, col.1, para.2; and p.533, col.2, "Accessibility steady-state body-voltage estimation"), and probabilistic analysis (see Shepard, p.533, col.2, section 3.2, para.1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard because while both Chuang and Shepard teach that the body voltage modulations are due to coupling effects, Shepard's model "allows one to determine the body voltage and its associated uncertainty, depending on knowledge of the switching activity of the FETs in question." (Shepard, p.538, col.1, para.2).

**38. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Chuang in view of Shepard_2.**

39. In regards to Claim 18,

18. The method of claim 16, wherein said electrical property comprises noise and said measuring step comprises measuring noise on one or more nets in said circuit as a constituent simulation for static noise analysis.

Chuang teaches that "The body voltage is modulating during the switching event due to the gate-to-body and diffusion-to-body coupling;

and thus only a transient analysis can properly model these coupling effects" (see Chuang: Abstract).

However, Chuang does not expressly teach measuring noise on one or more nets in a circuit as a constituent simulation for static noise analysis.

Shepard-2 teaches that "To check an entire digital integrated circuit with tens of millions of transistors for noise stability by means of dynamic simulation is not practical. Instead, static analysis techniques which couple simulations on groups of CCC's with a path trace are used." (see Shepard_2: p.1138, col.1, section IV, 1st para.).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Chuang with those of Shepard_2 because the technique in Shepard_2 "enables practical checking of noise stability on a chip-wide basis, assuming the worst allowable noise that might be acting in each circuit from all possible noise sources." (see Shepard_2: p.1138, col.1, section IV, 1st para.).

***Re: Applicant's 37 C.F.R. §1.131 Declaration***

40. Examiner finds Applicant's Declaration Pursuant to 37 C.F.R. §1.131, filed 12/4/2003 to be defective.

41. In the declaration, Applicant declares (para.2) that

> The inventions of claims 1-8 and 12-22 of the above-identified patent application, among others, were conceived and reduced to practice in this country, prior to April 19, 1999 (Henceforth referred

to as the "Critical Date"), which is the filing date of Chuang et al. U.S. Patent Application Publication No. US 2003 / 0078763.

42. Examiner agrees with Applicant that the two exhibits presented with the Declaration provide evidence of a date of conception. However, Examiner respectfully disagrees with Applicant's argument that these exhibits provide evidence of reduction to practice and due diligence. Applicant is referred to MPEP §715.07(III), which states that:

> A conception of an invention, though evidenced by disclosure, drawings, and even a model, is not a complete invention under the patent laws, and confers no rights on an inventor, and has no effect on a subsequently granted patent to another, UNLESS THE INVENTOR FOLLOWS IT WITH REASONABLE DILIGENCE BY SOME OTHER ACT, such as an actual reduction to practice or filing an application for a patent. *Automatic Weighing Mach. Co. v. Pneumatic Scale Corp.,* 166 F.2d 288, 1909 C.D. 498, 139 O.G. 991 (1st Cir. 1909).
>
> ... In general, proof of actual reduction to practice requires a showing that the apparatus actually existed and worked for its intended purpose. However, "there are some devices so simple that a mere construction of them is all that is necessary to constitute reduction to practice." *In re Asahi / America Inc.,* 68 F.3d 442, 37 USPQ2d 1204, 1206 (Fed. Cir. 1995) (Citing *Newkirk v. Lulejian,* 825 F.2d 1581, 3USPQ2d 1793 (Fed. Cir. 1987) and *Sachs v. Wadsworth,* 48 F.2d 928, 929, 9 USPQ 252, 253 (CCPA 1931). The claimed restraint coupling held to be so simple a device that mere construction of it was sufficient to constitute reduction to practice. Photographs, coupled with articles and a technical report describing the coupling in detail were sufficient to show reduction to practice.

43. Examiner finds that that Applicant's allegation that "the inventions of claims 1-8 and 12-22 ... were ... reduced to practice in this country prior to April 19, 1999" is a conclusory statement that is not supported by the exhibits.

44. Because the Declaration does not provide evidence of reduction to practice and due diligence, Examiner is maintaining the rejections based on the Chuang et al. reference.

***Re: Applicant's Response to 37 C.F.R. §1.105***

45. Examiner finds that Applicant's Response to the Requirement to Submit Information under 37 C.F.R. §1.105, filed on 6/28/2004, did not sufficiently respond to the questions raised in the §1.105 (dated 2/24/2004). The issues were lettered (a) – (g).

46. Issues (a) and (e) of the §1.105 pertained to Mr. Kim's role in the authorship of Exhibit A in the §1.131 declaration, and to Mr. Kim's role in the inventorship of the present application. The response to the §1.105 contains attorney arguments regarding the role of Mr.Kim. It appears that this was an attempt to submit a "Katz Declaration", as described in MPEP §2132.01. However, such a declaration must be signed by the Applicant and not by the attorney. Therefore, the attorney arguments are unpersuasive. MPEP §705.07(I) states that "Facts, not conclusions, must be alleged."

47. In regards to issues (f) and (g) of the §1.105, regarding IBM's grant, and IBM's possible rights to the invention, Applicant provided an Exhibit accompanying the response of 6/28/2004, which, in the final paragraph of the last page, refers to "a gift from the IBM Corporation under the

University Partnership Program". Applicant argues in the Response to the §1.105 that this gift program "disallows" IBM from patent ownership rights.

48. Examiner finds Applicant's arguments regarding issues (f) and (g) to be persuasive.

49. In regards to issues (b), (c), and (d) of the §1.105, Examiner finds Applicant's arguments to be persuasive.

***Conclusion***

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Correspondence Information***

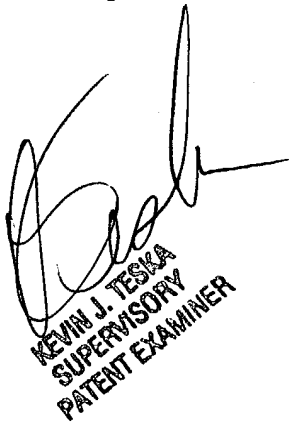
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone numbers are (703) 306-0297 *[Before Oct. 25, 2004]* and (571) 272-3714 *[After Oct. 25, 2004]*. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (703) 305-9704 *[Before Oct. 25, 2004]* and (571) 272-3716 *[After Oct. 25, 2004]*.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (703) 305-3900 *[Before Oct. 25, 2004]* or (571) 272-2100 *[After Oct. 25, 2004]*.




Ayal I. Sharon

Art Unit 2123

September 28, 2004